

[AN ESD PROTECTION POWER CLAMP FOR SUPPRESSING ESD EVENTS OCCURRING ON POWER SUPPLY TERMINALS]

Abstract

An ESD protection power clamp for suppressing ESD events. A clamping transistor having power source connections connected across the power supply terminals of an integrated circuit is connected to clamp the voltage during an ESD event. An RC timing circuit defines a time interval where ESD voltage for triggering the FET out of conduction. An inverter circuit connects the RC and timing circuit to the clamping FET. A dynamic feedback transistor is connected in series with one stage of the inverter and the power supply. During an ESD event, the feedback transistor delays the time for disabling the FET transistor, providing increased immunity against mistriggering of the clamping transistor, and forces the circuit to reset following the mistrigger event.